

Fig. 1

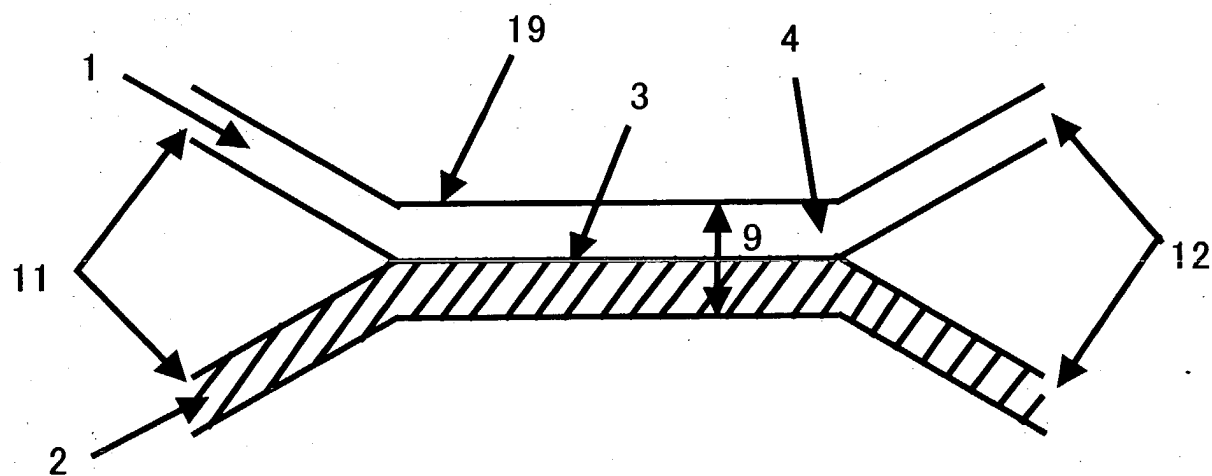
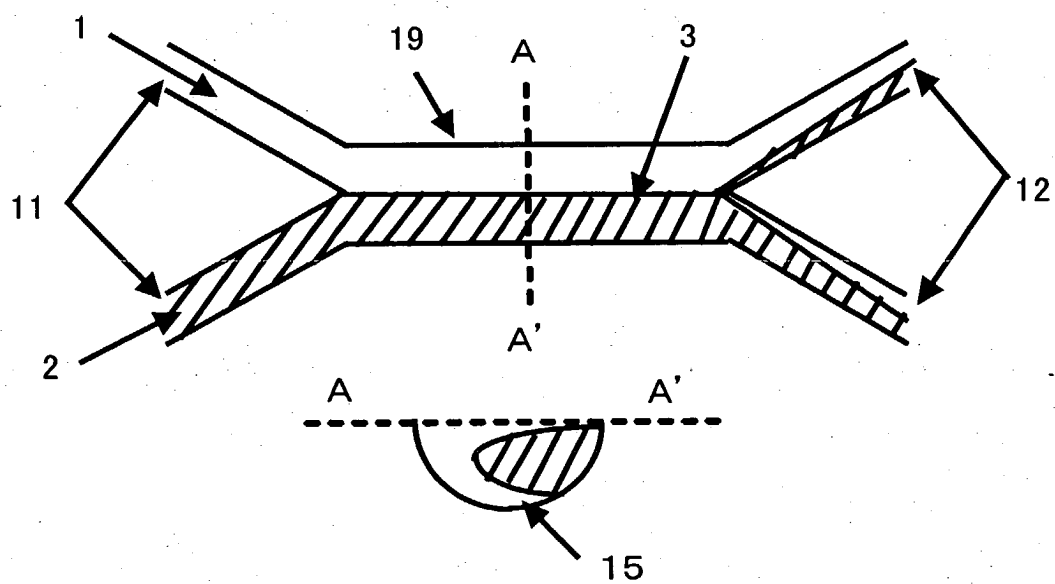
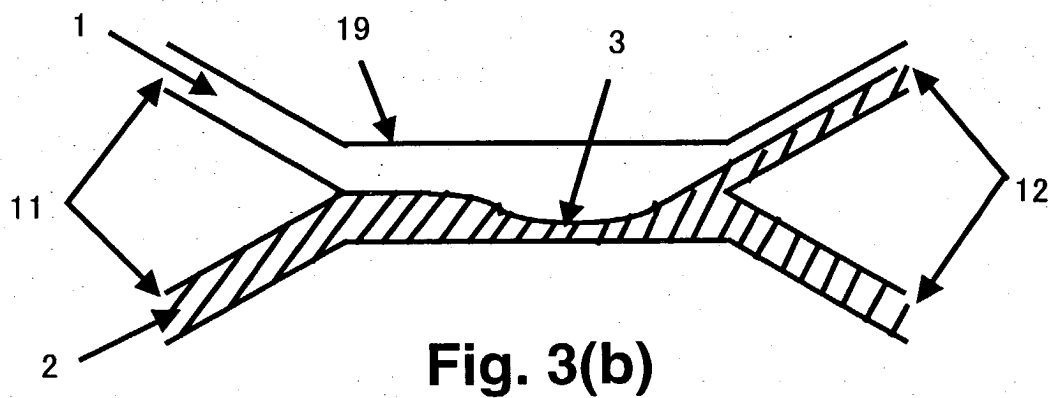
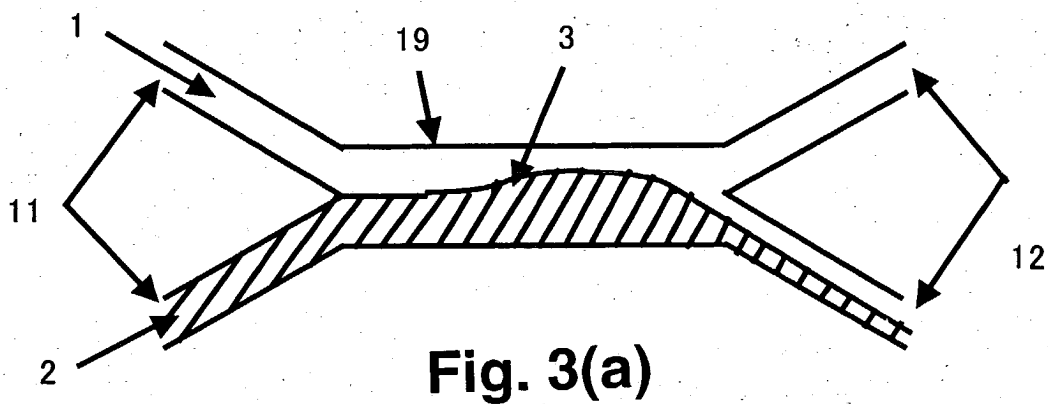


Fig. 2



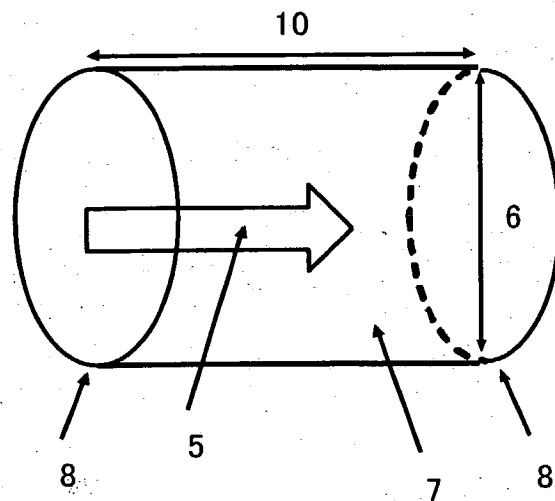


Fig. 4(a)

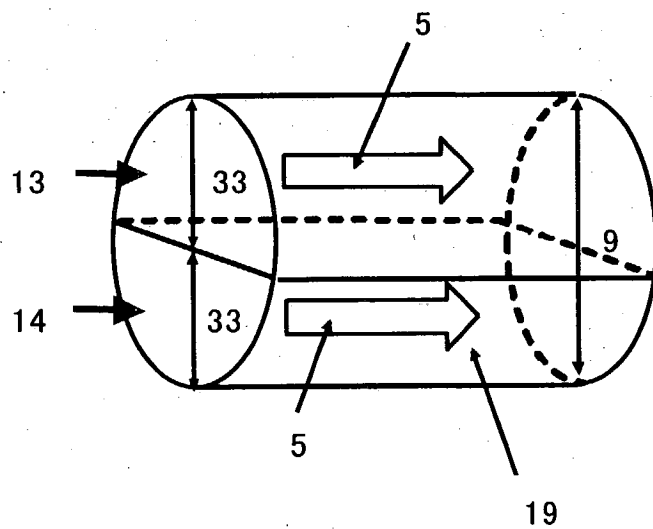


Fig. 4(b)

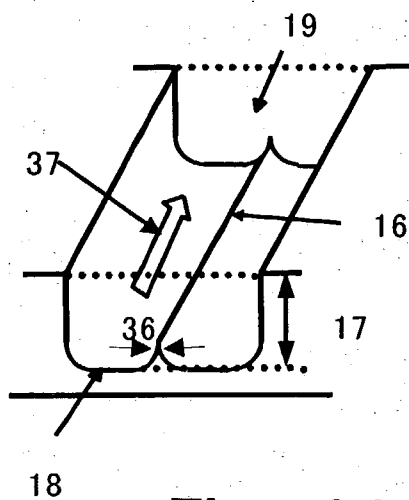


Fig. 5(a)

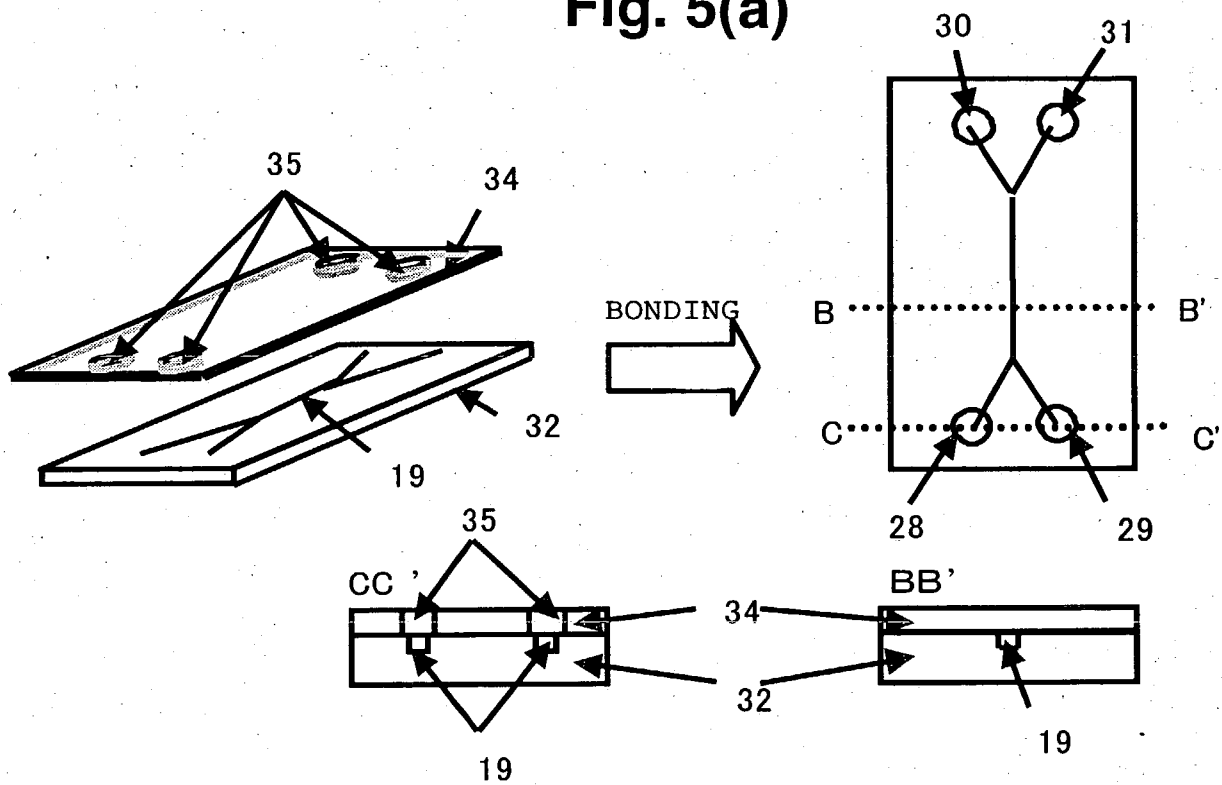


Fig. 5(b)

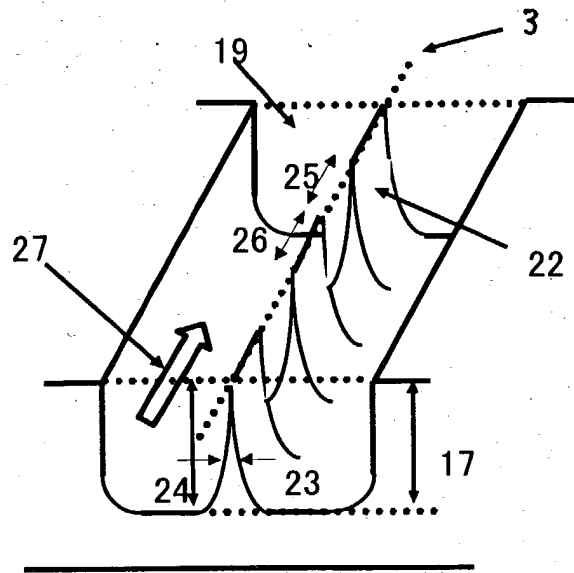


Fig. 6(a)

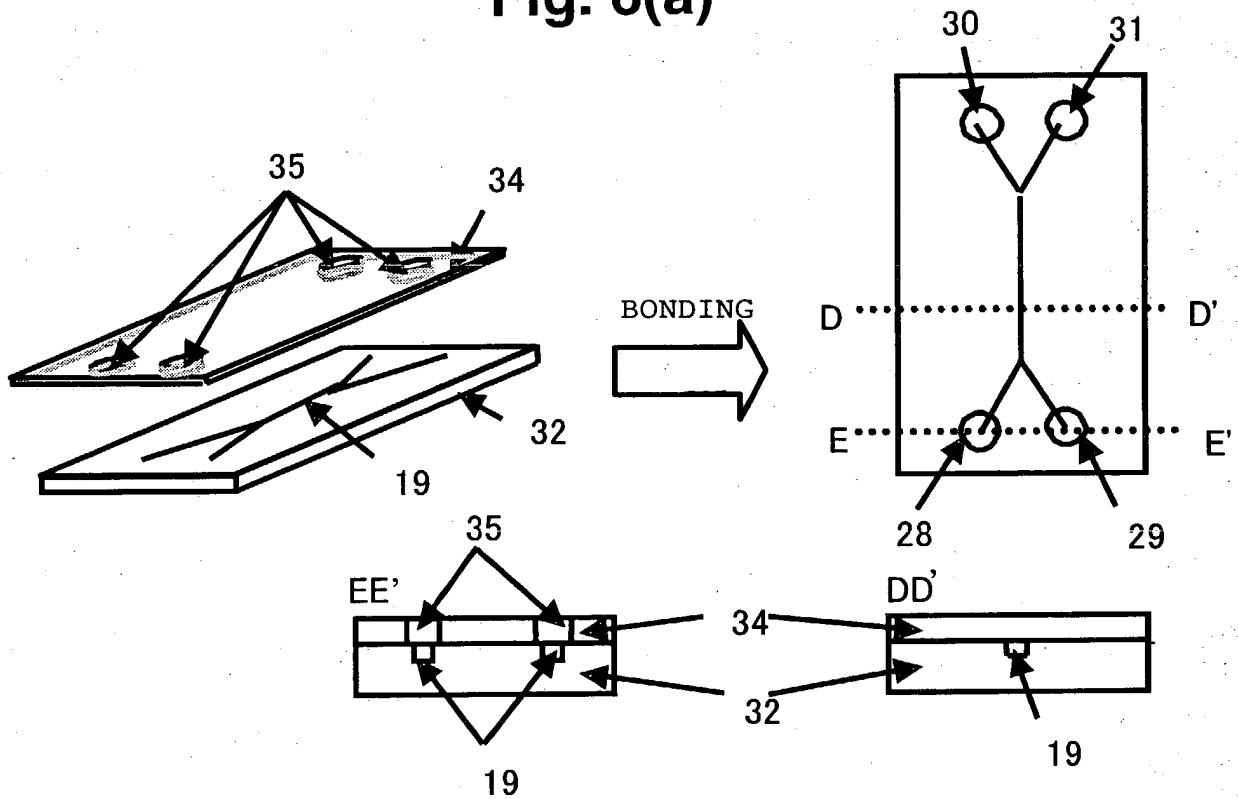


Fig. 6(b)

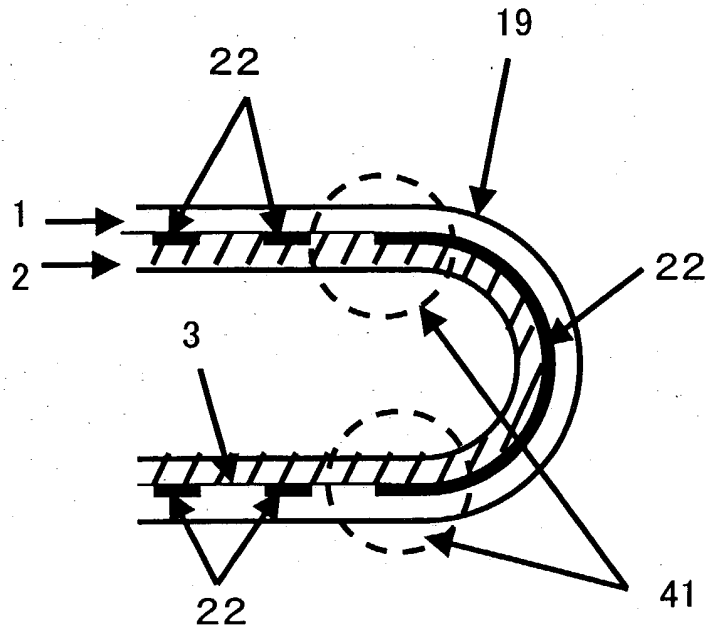


Fig. 7

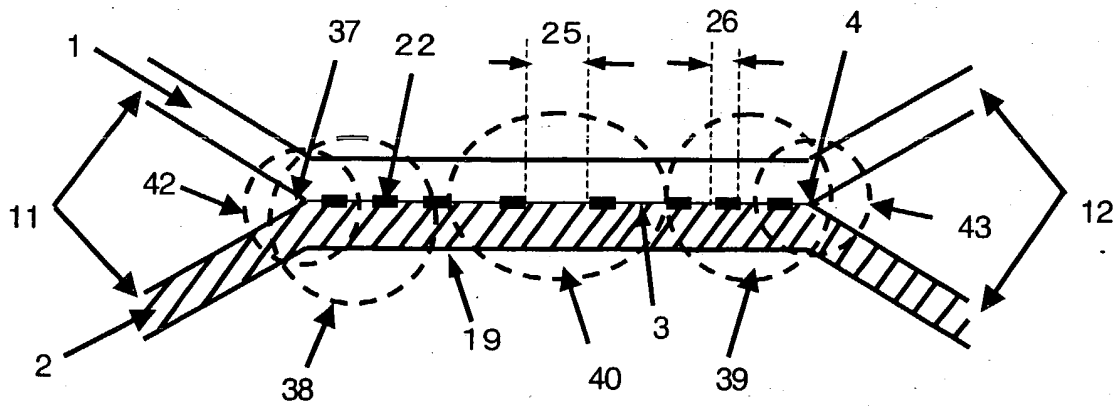


Fig. 8(a)

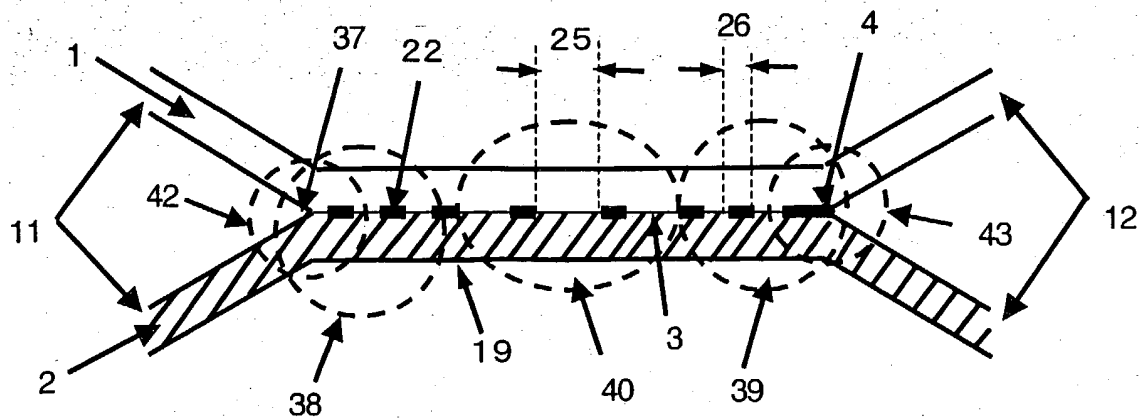


Fig. 8(b)

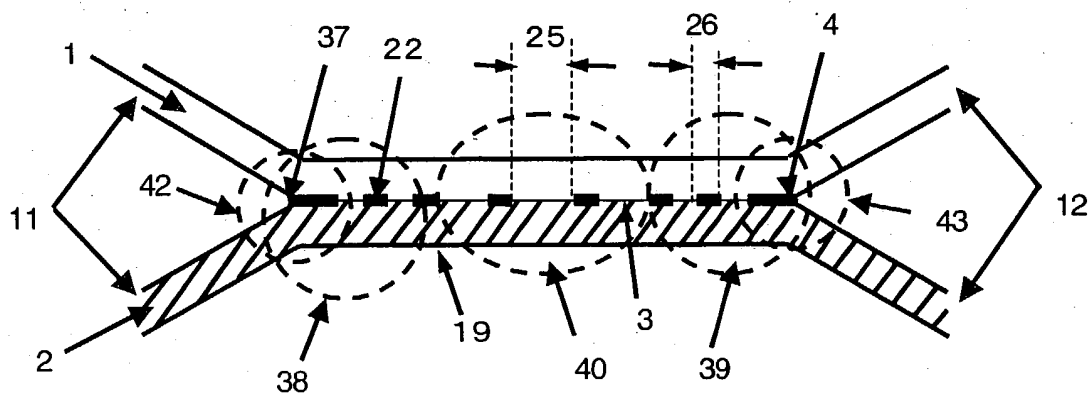


Fig. 8(c)

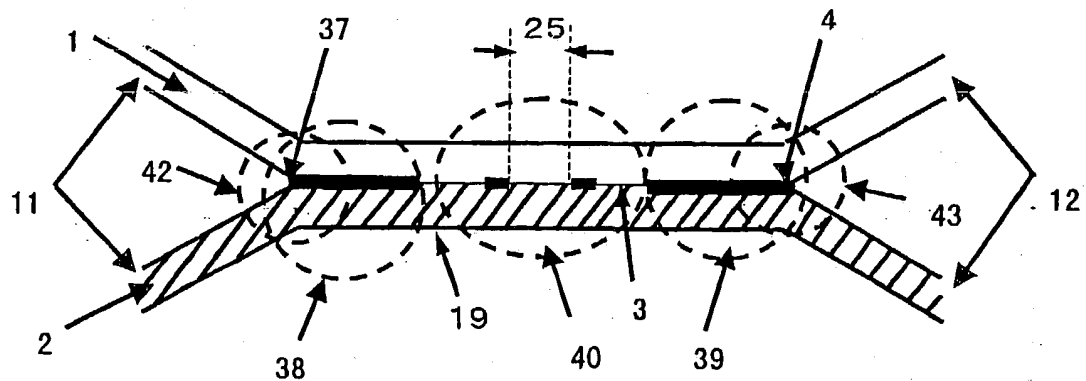


Fig. 8(d)

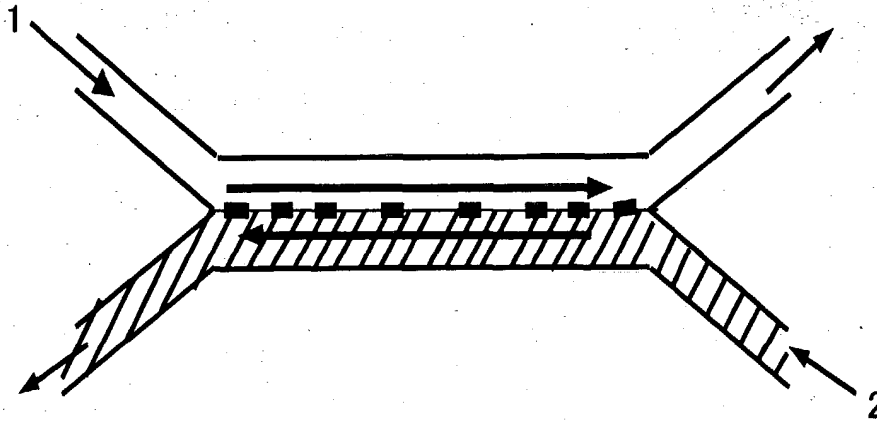
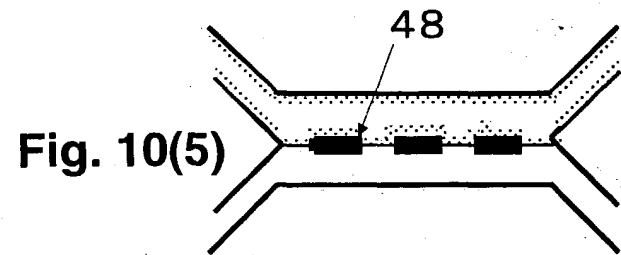
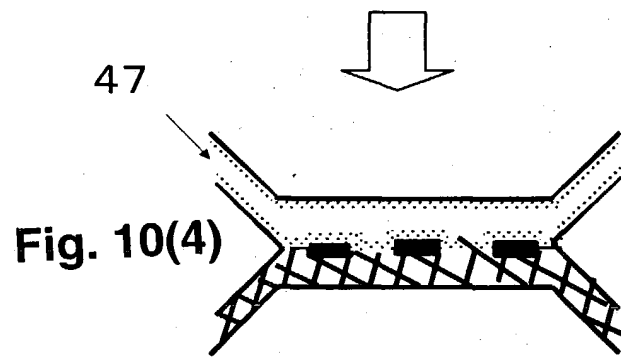
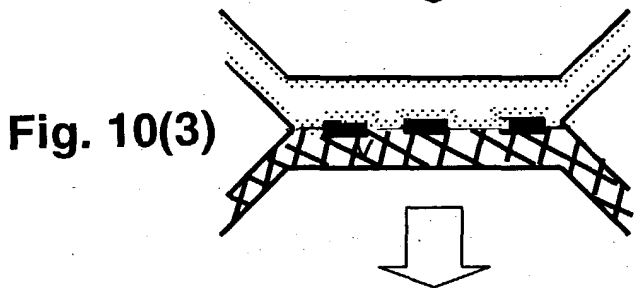
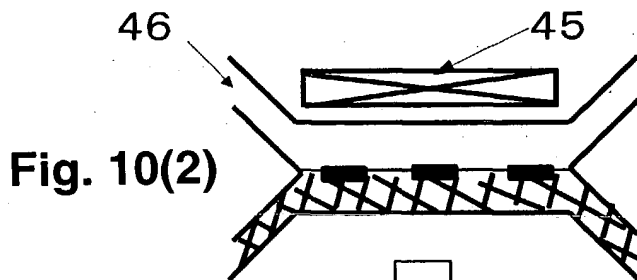
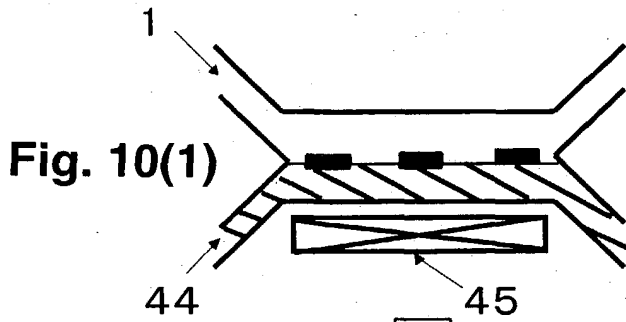


Fig. 9



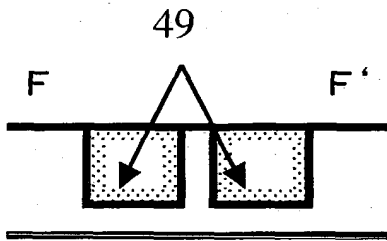
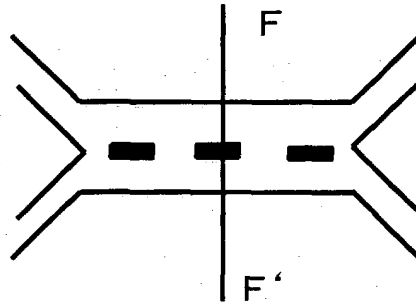


Fig. 11(a)

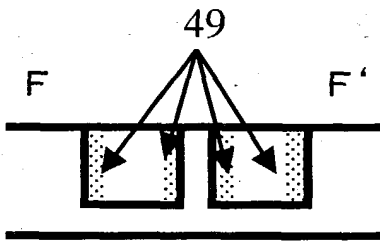


Fig. 11(b)

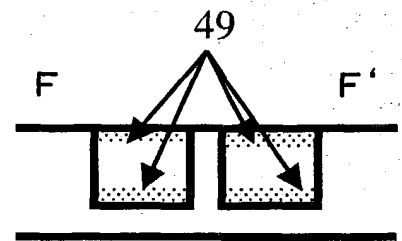


Fig. 11(c)

Fig. 1 is a schematic cross-sectional view of a semiconductor device. It shows a substrate 18 with a layer 52 on top. A central region 50 is defined by a dashed line 20. A layer 19 is on top of 50, and a layer 22 is on top of 19. A layer 51 is on the right side of 50. Arrows point to the various layers and regions.

Fig. 12(d)

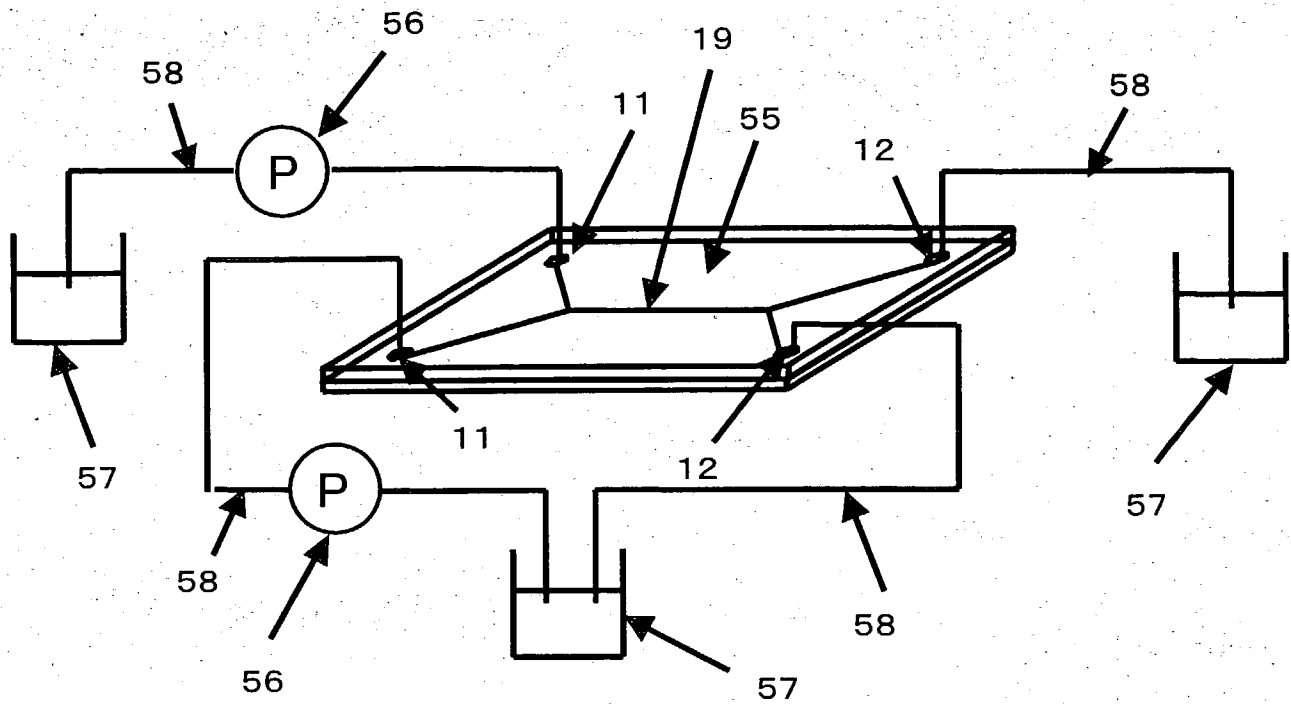


Fig. 13(a)

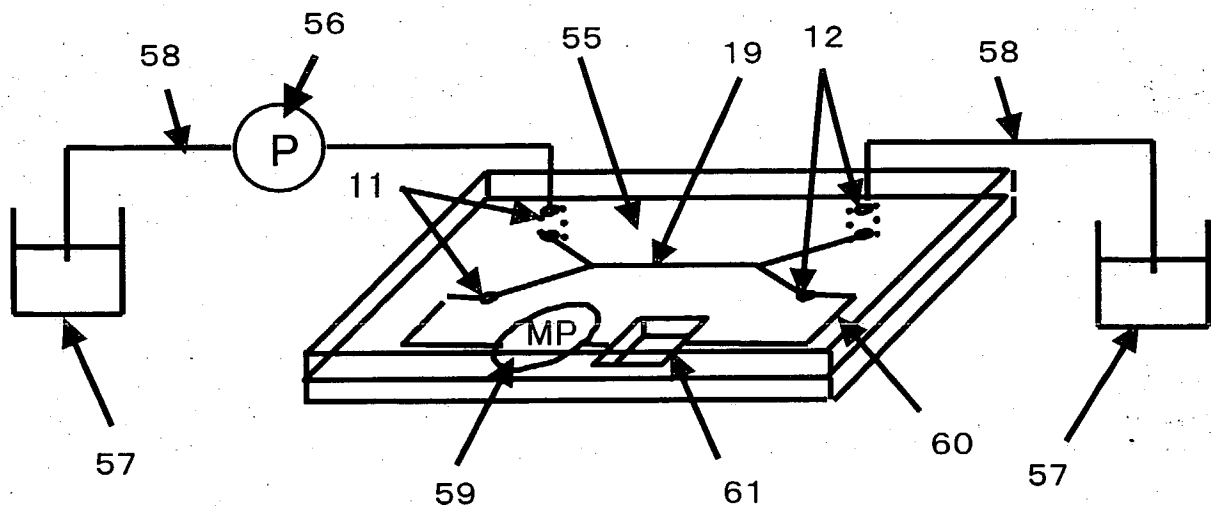


Fig. 13(b)

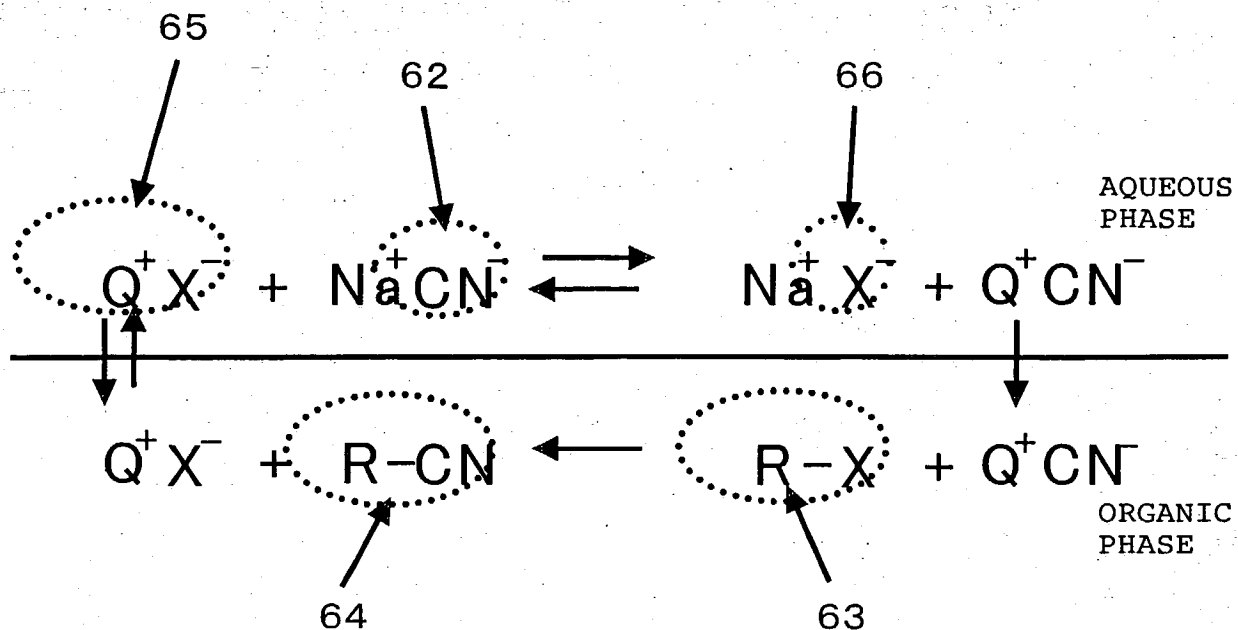


Fig. 14

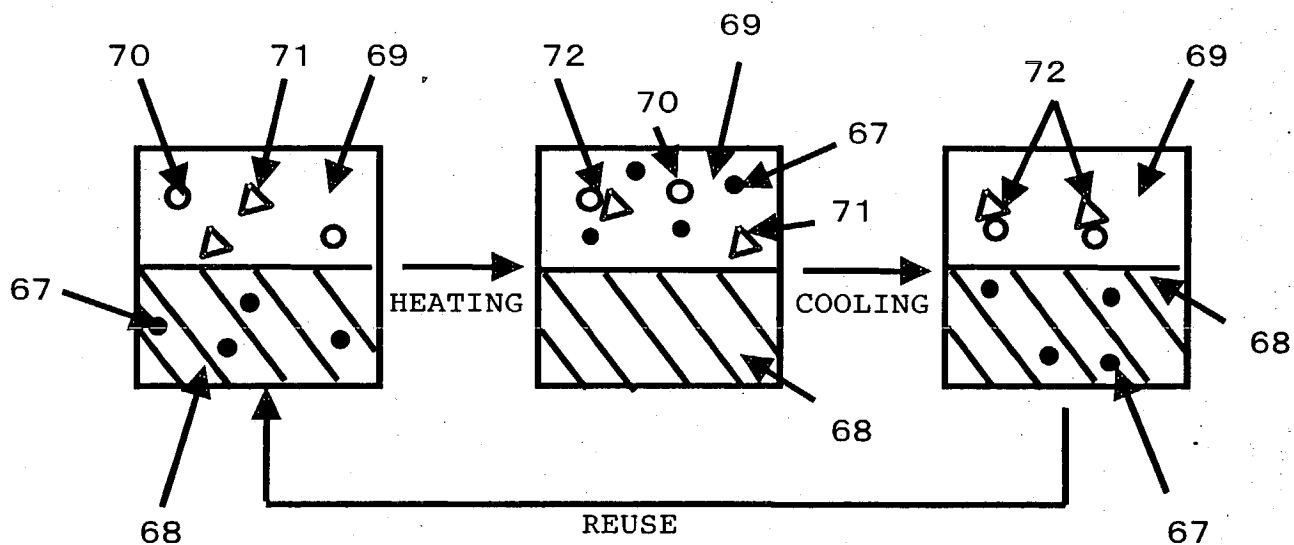
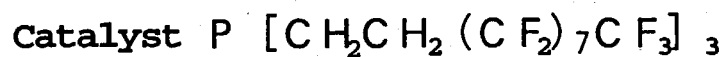
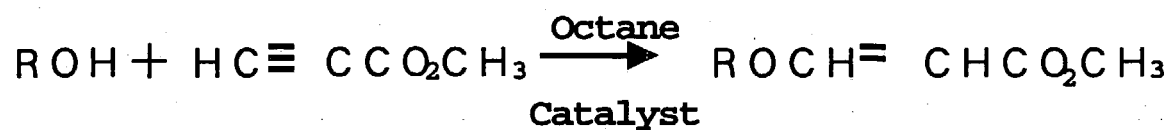
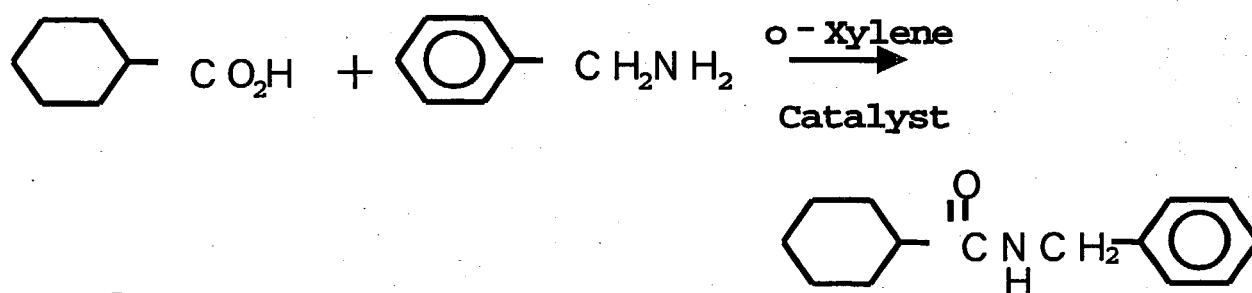


Fig. 15

G l a d y s z r e a c t i o n



Y a m a m o t o r e a c t i o n



Catalyst

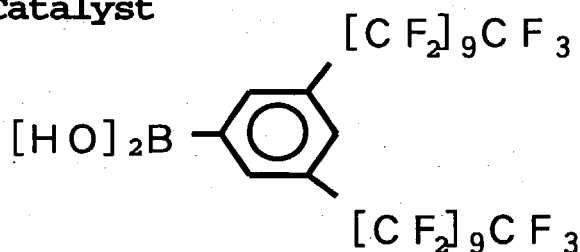


Fig. 16

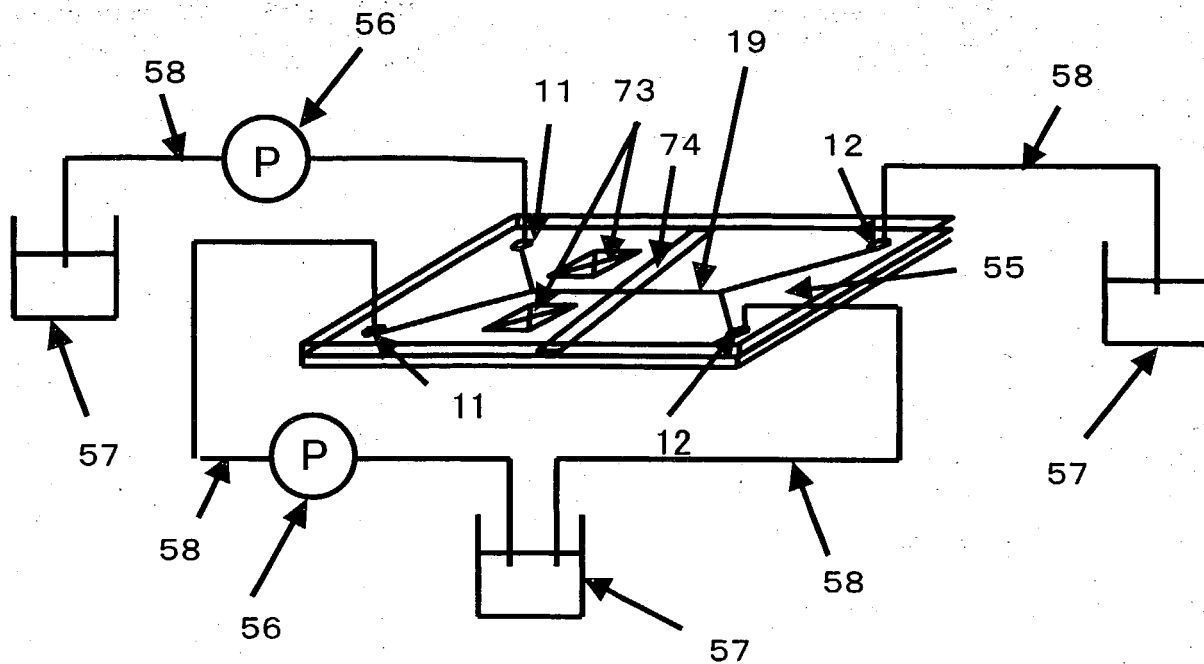


Fig. 17

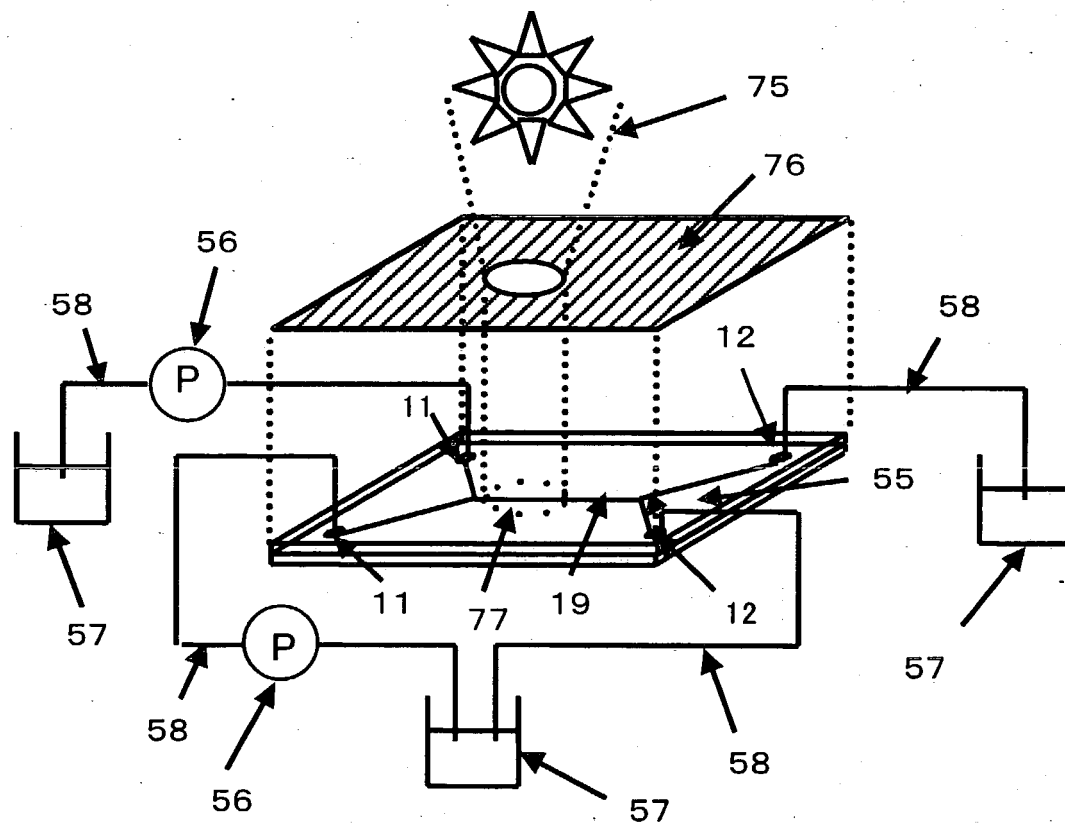


Fig. 18

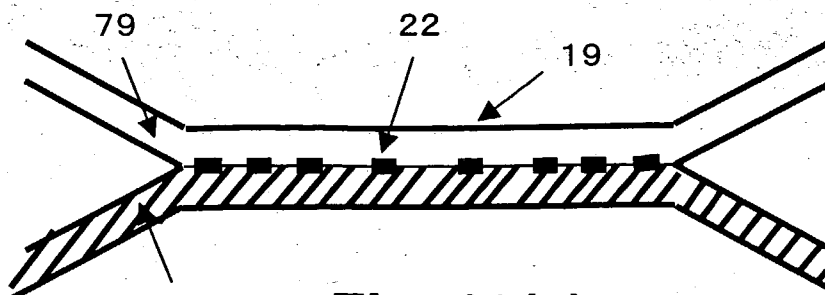


Fig. 19(a)

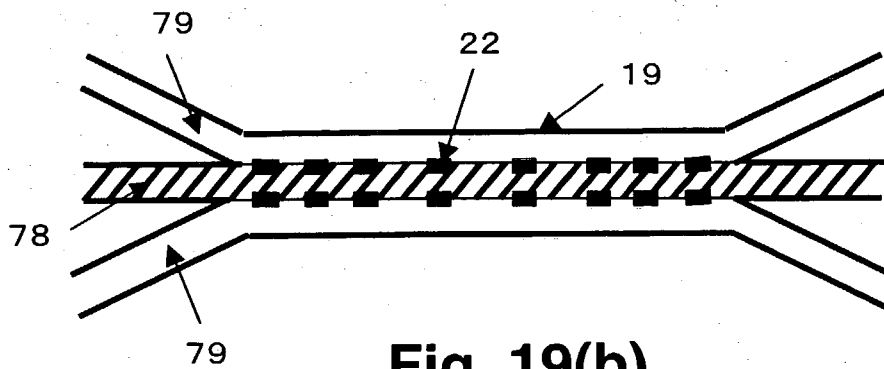


Fig. 19(b)

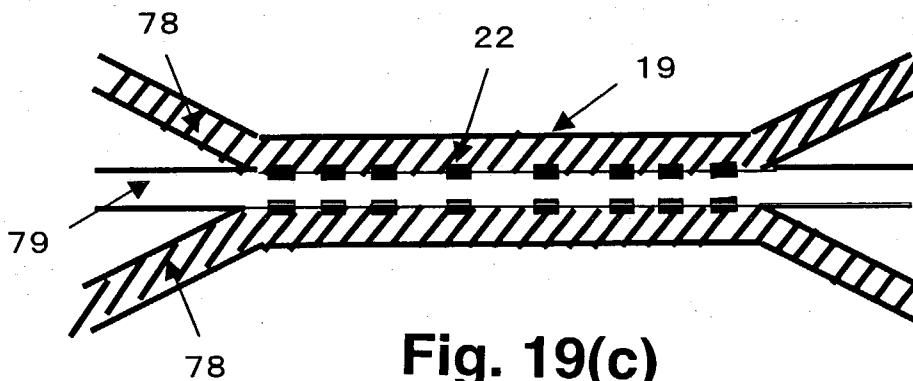


Fig. 19(c)

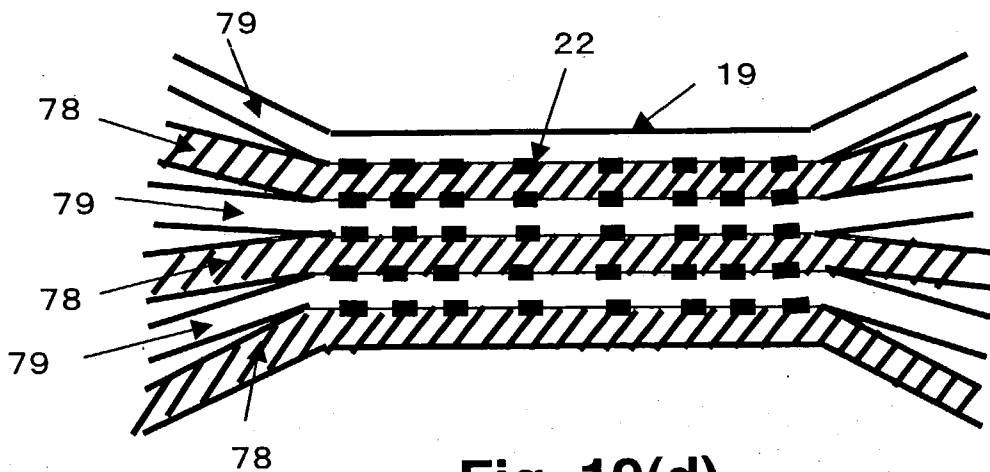


Fig. 19(d)

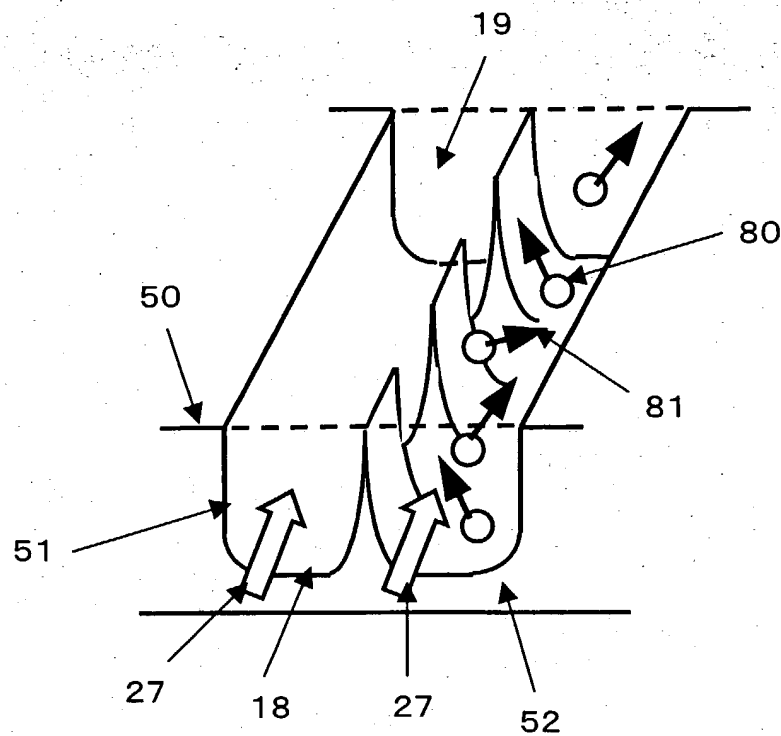


Fig. 20

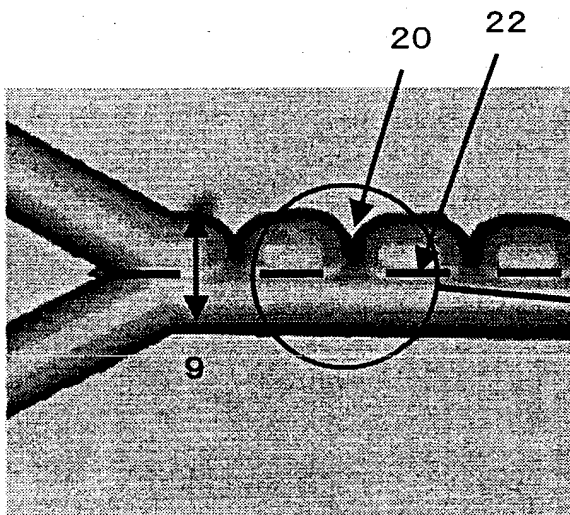


Fig. 21(a)

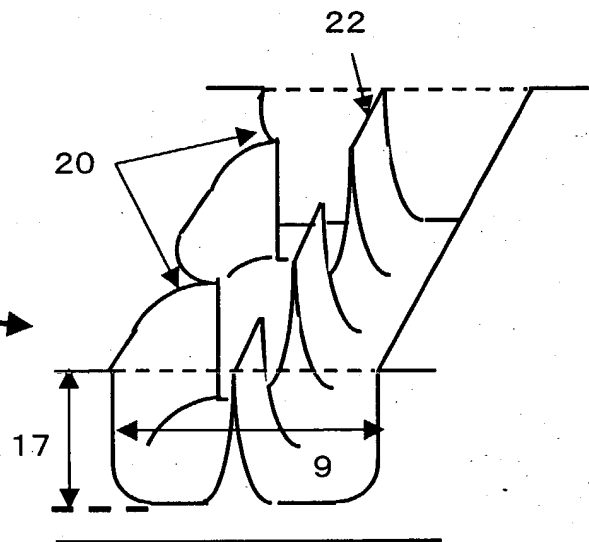


Fig. 21(b)

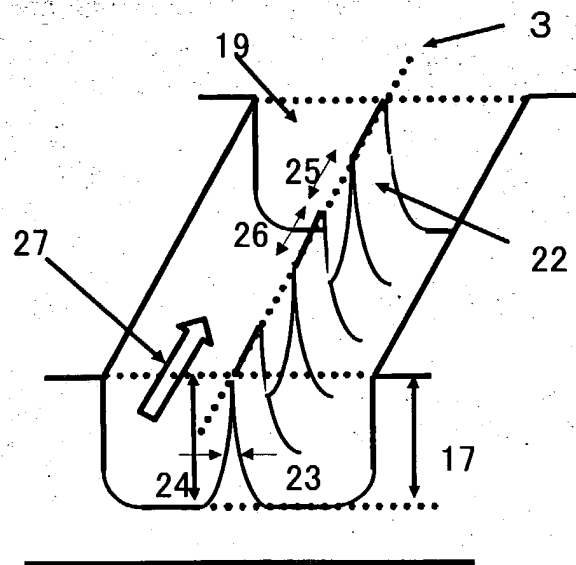


Fig. 22(a)

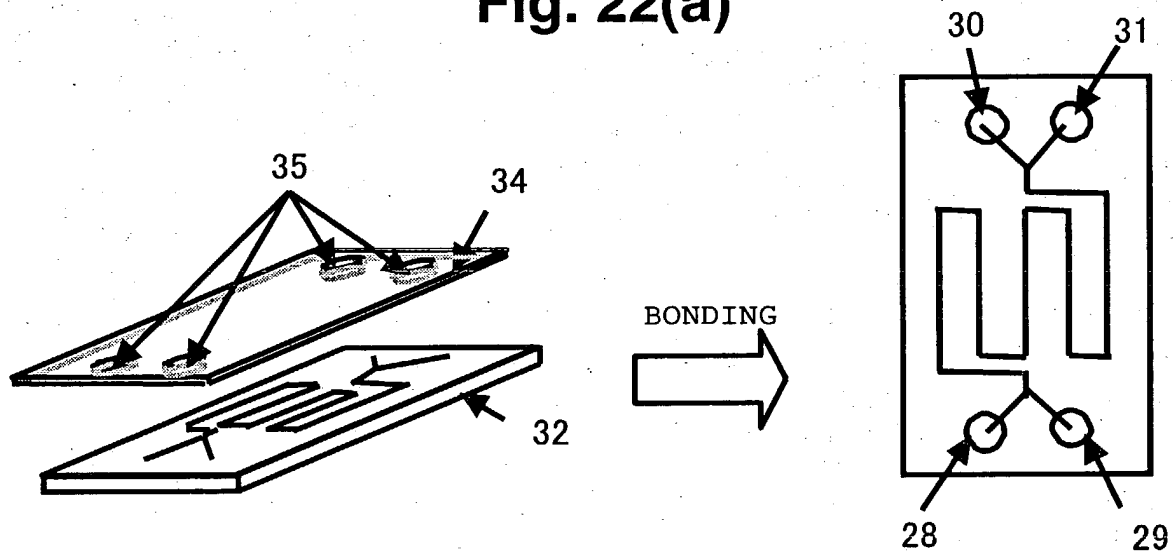


Fig. 22(b)